# PATENT SPECIFICATION

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## (54) TWO-WAY DATA TRANSMISSION SYSTEM FOR CABLE TELEVISION NETWORK

(71) We, RAI RADIOTELEVISIONE ITALIANA, of Viale Mazzini 14, Roma, Italy, an Italian Body Corporate, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a method and a device for establishing two-way communication between a central unit and a plurality of subscriber terminals of a cable television (CATV) system.

An object of the invention is to offer to the cable television subscribers, in addition to the several broadcast television programmes, the opportunity of sending information back to the central unit, information which may be, for example, answers to poll questions carried out about a television programme by the central unit. The subscribers may thus take part in the TV programmes, with a quick collection of the opinions of the subscribers for educational, statistical or other purposes being achieved.

The system of the invention also offers other services to the subscribers, such as taxed programmes, meter-reading, teletypewriters, and so on.

It is a feature of the proposed system that the polling is sent by the central unit and is received by all subscribers almost simultaneously.

The answers of the subscribers, prepared by means of a keyboard, one for each subscriber, are sent sequentially to the central unit where they arrive one after another without a noticeable time interval between them, according to a prefixed programme. This is achieved by generating in each subscriber equipment an "answer delay" which is different for each subscriber. In this way, a more rapid collection of answers is obtained than with systems which sequentially poll one subscriber at a time.

According to this invention there is provided a method of establishing two-way electrical communication in a cable television system between a central unit and subscriber terminals, the method comprising:— (i) transmitting information in the form of a data stream from the central unit to a plurality of subscriber terminals simultaneously, the data stream including timing information for establishing a fast clock and a slow clock at each terminal, the slow clock having a period which is a multiple of the fast clock period, the data stream also including a reset signal, an answer format signal, and command signals; (ii) at a subscriber terminal receiving the data stream, identifying the reset signal, delaying the data stream, and counting pulses of the slow clock starting from the answer format signal to generate a time delay characterising the said terminal; (iii) generating, at a keyboard associated with the said terminal, a subscriber's answer to information in the received data stream; and (iv) transmitting the answer from the said terminal to the central unit, the time interval between the receiving of the reset signal and the transmitting of the answer being determined by the characteristic time delay, each subscriber terminal having a different time delay assigned to it such that answers from the terminals are received at the central unit one after another in time-division-multiplexed form.

Also according to this invention there is provided a subscriber terminal device connectable to a cable television system for two-way electrical communication, in which system a data stream having a fast clock bit time interval and including synchronising words at a slow clock interval, a reset signal, an answer format signal, and command signals are generated at a central unit and are transmitted to the terminal device, answers from the terminal device being received by the central unit,

the terminal device comprising:— first regenerator means for regenerating the fast clock pulses; shift register means controlled by said first regenerator means for receiving the data stream from the central unit and generating a delay corresponding to the expression $2(T_{max}-T_j)$, wherein $T_{max}$ is the time taken for the data stream from the central unit to reach a remote subscriber, and $T_j$ is the time to reach the particular terminal device; word decoder means connected to the output of said shift register means; second regenerator means controlled by said shift register means for regenerating slow clock pulses; counter means for receiving said slow clock pulses and for counting up to a number J assigned to that terminal device, said counter means beginning the count of slow clock pulses when the answer format signal from the central unit is received and decoded by said word decoder means; and keyboard means for entry thereon of answer data, said counter means producing an output gate upon reaching the count of said number J for enabling the transmission of the answer data from the terminal device.

If $T_j$ is the propagation time for an electric signal travelling between the central unit and a group of subscribers connected to a branching amplifier j, and $\tau_r$ is the duration of each answer message, then, for the answer messages to arrive at the central unit sequentially, the generated answer delay $R_j$ at a subscriber terminal J is given by:—

$$R_j=2(T_{max}-T_j)+J(\tau_r+\Delta t) \qquad (1)$$

where $T_{max}$ is the time taken for the signal to reach the most remote amplifier, and $\Delta t$ is the tolerance which takes into account the double delay due to the cable connecting the branching amplifier and the subscriber terminal.

The delay $R_j$ is generated at the subscriber terminals in the following way: the central unit sends to the subscriber terminals timing information from which two clock signals are generated, of which one is fast rated and has a period $t_0$, and the other is slow rated and has a period $(\tau_r+\Delta t)$ which is a multiple of $t_0$.

The first term of the delay $R_j$ in equation (1) is generated by a shift register (operated by the clock of period $t_0$). The pulses at the output of the shift register are fed to a word decoder from which the "count beginning" command signal, the slow clock signal and the reset signal are obtained. A counter counts J pulses of the slow clock before allowing transmission of the answer message prepared by the subscriber.

In this way, by keeping $t_0$ constant and by varying the slow clock $(\tau_r+\Delta t)$, the "answer plan", that is the allocation and the contiguousness of the subscribers' answers, is performed.

In the preferred embodiment the signal sent towards the subscriber has the form of a continuous bit stream, with period $t_0$ organised in "words" each containing 8 bits. The information is coded by employing combinations which have 2 or 4 bits with logic value 1 (except the four combinations 11000000, 00000011, 11110000 and 00001111, which could be incorrectly read). In this way, for each word, 94 combinations are available, of which 10 are employed by the subscriber's terminal to carry out the following operations:—

S: a synchronisation word correlated to the slow clock whose period is $(\tau_r+\Delta t)$ and necessary to define, by means of the subscriber counter, the sequence of answers (answer plan);

A: reset word (cancels all commands stored in the memory of the subscriber terminal, and sets the subscriber counter to zero);

F: word specifying the answer format ($F_1$=anonymous answer; $F_2$=answer with address);

$B_1 \ldots B_8$: command words to the subscriber's terminal specifying the type of answer, for example:—

a) anonymous answer with short message (yes-no-I don't known) typical of participation systems;

b) automatic answer with subscriber's address, which may be used for pay television programmes, reading of meters, alarms, and so on;

c) manual answer with subscriber's address, which may be used for purchases ordered from the purchaser's house, voting, educational systems, and so on.

In one embodiment of subscriber terminal in accordance with the invention, the word decoder comprises:— first and second serially connected shift registers, having respective 64 and 8 delay stages, which registers feed a first diode matrix, a parity check circuit and separator means, the latter being connectable to external equipment; an "EXCLUSIVE OR" circuit connected to receive signals from the input of the first shift register and from the last output of the second shift register, the output of the said "EXCLUSIVE OR" circuit being connected to the input of a third shift register comprising seven delay stages; an "AND" gate connected to receive signals from the outputs of the third shift register and the output of the parity check circuit; and a second diode matrix connected to receive signals from the output of the "AND" gate, from the output of the parity check circuit and from the

outputs of the second shift register, for decoding the words and commands of the incoming data stream; the word decoder further comprising bistable flip/flops of the set/reset type for storing the decoded commands.

The subscriber terminal makes use of a clock of fixed period $t_0$ to generate the time interval ($T_{max}-T_j$) which determines the delay $R_j$ (see equation (1)). This clock is also used by the subscriber terminal for the return message which has the form of a continuous bit stream, with period $t_0$ organised in "words" each containing 8 bits.

The reset A, the commands $B_1 \ldots B_8$, and the format F are transmitted to the subscriber at the beginning of each polling cycle, and are then repeated 9 words later in order to increase the reliability of the system. The reset A is repeated four times.

Eight words remain available between two synchronising signals S, except in the interval at the beginning of the polling cycle, when the reset, the command B and the format F are transmitted. That interval is however of negligible duration.

These available "words" may be employed for further services directed to all subscribers, such as for instance for driving teletypewriters, for facsimile transmission, and so on, or for information directed exclusively to one particular subscriber, either by singling him out by means of his address, or by fusing the feature of this system, without the need to employ a special address.

Thus the answer messages of the subscriber sent to the central unit are of two kinds: anonymous short messages, and long messages with the subscriber's address.

In the preferred embodiment the message forming the subscriber's answer, encoded in baseband with a NRZ (non-return to zero) code, is transmitted towards the central unit in FSK (frequency shift key) modulation within a band ranging from 5 to 30 MHz, whereas the stream directed towards the subscribers is transmitted, in FSK modulation, within the band 50 to 300 MHz. Transmitting the messages to and from the central unit in different frequency bands requires the use of only a single transmission cable between each subscriber and the central unit. However, in an alternative embodiment two cables are provided between each subscriber and the central unit, the outward and return messages being transmitted in baseband on separate cables.

In the central unit, the centralised equipment transmitting towards the subscribers includes a processor with conventional peripheral units, chosen with a capacity adequate for the expected number of subscribers. When suitably programmed, the processor may carry out the following operations:—

memorising and updating the central unit subscriber directory in response to input data (addresses of new subscribers, address changes and subscriber's withdrawals);

providing the installing personnel with the data necessary for correct insertion of the subscribers in the "answer plan";

generating the messages to be transmitted towards the subscribers in response to a specific request or to an internal programme; and

receiving the messages from the subscribers, comparing them with the memorised "answer plan" by checking the timing of each subscriber answer (in case of addressed messages), and memorising the answers for subsequent operations;

for some services, arranging and processing in real time the input data, and supplying the results to peripheral devices (displays, printers, alarms, and so on); and

detecting anomalous behaviour with respect to the answer plan, and informing the maintenance personnel of the addresses of the subscribers whose equipment is out of order or is presumed to be out of order.

The main tasks of the subscriber's terminal are: generating the answer delay, generating the answer through the subscriber's keyboard, and extracting ancillary signals for teletypewriters, facsimile, video displays, etc., and for further services, if any.

The invention will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 is a basic block diagram of a part of a subscriber terminal;

Figure 2 schematically shows the data stream transmitted by the central unit towards the subscribers;

Figure 3 is the scheme of the subscriber's answer in the case of a short message;

Figure 4 is a similar scheme in the case of a long message;

Figure 5 is a more detailed block diagram of the subscriber terminal;

Figure 6 is a block diagram of the delay stage preceding the word decoder in Figure 5;

Figure 7 is a block diagram of a preferred embodiment of the word decoder;

Figure 8 is a block diagram of a preferred embodiment of the block "divider and subscriber counter";

Figure 9a is a plan of a subscriber counter circuit card;

Figure 9b is a side elevation of a group of several such cards determining the subscriber's number; and

Figure 10 is a block diagram of a

preferred embodiment of answer message generator.

Signals received by the subscriber terminal from the central unit are demodulated and then, as is shown in Figure 1, fed to a circuit 2 for regenerating the fast clock with period $t_0$ and to a shift register 3 controlled by the fast clock; the regenerating circuit is connected to the word decoder 4 and the shift register is connected to the same decoder 4 and to the slow clock regenerator 5.

The outputs of the word decoder and of the slow clock regenerator are connected to the subscriber counter 6 which is connected to the circuit 7 for generating the subscriber's messages, which in the preferred embodiment is a keyboard with logic circuits of known type.

The data stream received by the terminal is in the form of a series of 8-bit words. In Figure 2 each letter or space represents an 8-bit word, the meaning of which is as follows:—

S denotes the synchronising word,

A denotes the reset word,

B is a command word sent from the central unit to the subscriber terminal in order to preset the type of the required answer;

F is a word which specifies the answer format;

␣ denotes a word which may be used for other ancillary services.

Figure 3 shows how the various bits are used for the short answer from the subscriber terminal towards the central unit. These bits are the following:—

Starting sequence: 4-bit sequence with logic value 1010. This serves to carry out a phase control in order to locate correctly at the centre of the demodulation window the reading clock in the receiver of the central unit. A frequency reference is not necessary since the fast clock at the subscriber terminal is locked to the data stream received from the central unit.

Beginning of the answer: 8-bit sequence 01111110 the recognition of which defines the beginning of a subscriber's answer.

Answer: this comprises numbers encoded in an "excess three binary decimal code". This code has been chosen in order that there shall be at least a logic level 1 in each group of four bits. The data comprise a 4-bit message generated by the subscriber's keyboard.

Figure 4 shows the use of the various bits for the long answer from the subscriber towards the central unit. The first 16 bits have the same function as the bits for the short answer (Figure 3); the subsequent bits comprise:—

receiving TV channel: a 4-bit sequence for identifying the TV channel employed by the subscriber at this moment (taxed TV programmes);

repetition of the received command: 4-bit sequence repeating the commands $B_1$ to $B_8$ received by the subscriber;

data from external equipments: a 16-bit sequence for coding data coming from external equipments (meter reading, alarms, etc.);

parity bits: a 4-bit sequence for the parity check of the message;

subscriber identifying number: a 20-bit sequence for transmitting the address (subscriber's number).

Figure 5, which shows the block diagram of the subscriber terminal, is now described.

The cable carrying the television signals and the data stream, enters a group of high-pass and low-pass filters; this group of filters, which is not a part of the system of the invention, has three outputs two of which are connected to the subscriber's terminal through the cables $C_1$ and $C_n$ and the other is connected to the television set for receiving the television programmes.

The signal received from the central unit (in the form of an FSK-modulated carrier) is sent to the FSK demodulator 1A whose output is connected to the fast clock regenerator 2A and the delay stage 3A. The delayed data stream is then fed to the word decoder 4A. The latter utilises the fast clock (period $t_0$).

The word decoder 4A, the structure of which is disclosed later on, carries out the following operations:—

recognition and extraction, from the data stream arriving from the central unit, of the synchronisation signal S, of the reset word A and of the answer format words $F_{1,2}$ necessary for correct operation of the divider and subscriber counter 5A;

recognition, extraction and storage of commands $B_1$ and $B_8$ which are supplied both to the answer message generator 6A, and through a suitable connector, to external equipments, if any;

sending to an external ancillary equipment, through a wire for each bit, the word sequence extracted from the data stream, the synchronisation word S, the parity check and the fast clock;

reading the word following the synchronisation word S which stops the counter, identification of the meaning thereof and sending this meaning to the display located on the control box 8A. To this end the decoder employs the pulses T and R with which it is supplied by the circuit 5A.

The word decoder has associated therewith the divider and subscriber counter 5A (the structure of which will be

described hereinafter) which carries out the following operations:—

regeneration of the slow clock from the fast clock, the synchronisation word S and the answer format words $F_{1,2}$;

generation of the subscriber's answer window after having counted a predetermined number (characterising that subscriber) of pulses from the slow clock (subscriber's delay);

generation of the number characterising the subscriber, and sending it to the "answer message generator" 6A;

generation of the timing pulses necessary to the "answer message generator" in order to allocate the bits and words forming the answer message of th subscriber as shown in Figures 3 and 4; and

generation of pulses R and T necessary for the storage of the information to be displayed.

The timing pulses from the divider and counter 5A, the commands $B_1$ to $B_8$ from the word decoder 4A together with the subscriber's answers coming both from the control box 8A and from external equipments, are supplied to the "answer message generator" 6A which allocates the single bits and the words of the message in the way shown in Figures 3 and 4.

The message formed in the answer message generator is sent to the FSK modulator 7A which transfers the coded message to two switched carriers whose frequencies are chosen according to the location which the data stream, returning from the subscriber towards the central unit, must have within the frequency bands allowed by the two-way cable television system. Transmission of an output signal occurs only during the predetermined "answer window" generated by the divider and counter 5A.

The modulated signal from the FSK modulator 7A is transmitted to the central unit via the attenuator 9A and the cable $C_u$.

The control box 8A has an answer keyboard for the subscriber and a display.

The control box preferably has keys for selecting the television channels and a control for the channel tuning of the television set.

The blocks 3A, 4A, 5A, 6A are shown in more detail in Figures 6 to 10.

Referring to Figure 6, which shows the block 3A in greater detail, the data stream is delayed in steps of value $t_e$ ranging from $t_0$ to 210 $t_e$ by means of shift registers which are interconnected by removable bridges. The shift registers are of a dynamic type; the biphase clock is obtained from the fast clock by means of a known circuit which matches the characteristics of the shift registers and is generally supplied from the manufacturer thereof.

Also the separators E are of known type, and may be necessary or not according to the characteristics of the shift registers.

Figure 7 shows in detail a preferred embodiment of the word decoder, the operation of which is as follows:—

Data, delayed by the block 3A (Figure 5), is sent to three serially connected shift registers, the first 1B, and the third 3B each having eight stages, the outputs of which feed the diode matrices 4B and 5B; the second shift register 2B, having 64 stages acts solely as a delay element. The first diode matrix 4B identifies the synchronising word S, the reset word signal A, the answer format words $F_1$ and $F_2$ and the command words $B_1$ to $B_8$; the second matrix, beside said words, identifies also the words following the synchronising word S.

Since the synchronising word S, the reset word A, the answer format words $F_1$ and $F_2$ and the command words $B_1$ to $B_8$ are repeated every nine 8-bit words, they will appear simultaneously at the inputs of both matrices, provided they have not been modified by noise in the CATV transmission system. The validity of the received data stream may be checked by comparing the two matrix inputs and also by means of the parity check circuit 6B.

The command words $B_1$ to $B_8$ are stored in bistables of the S/R type which form the commands memory 8B, and are sent both to the answer message generator and to any external equipments. The commands memory 8B is reset by the reset signal A.

The diode matrix 5B decodes the word following the synchronising signal S. Since this word is not repeated every 72 bits, the validity check is effected by the circuit 6B which checks the parity of the number of bits with logic value 1 (or 0) composing said word. The meaning of eight of these words is memorised employing the transfer pulse T, in bistables 9B of the S/R type (display memory); the memory 9B is reset by the pulse R. The timing of the signals T and R is derived from the timing of the "answer window" of the particular subscriber.

Figure 8 shows the preferred embodiment of the divider and subscriber counter block which operates as follows:—

The fast clock is fed to three synchronous dividers serially connected to each other, of which the first, 1C, divides by 8 and the others, 2C and 3C, divide by 3. The divider 1C provides the bit synchronisation (a, b, c) for the answer message generator. The second divider 2C feeds directly the demultiplexer 5C ($a_1$, $b_1$) the third one 3C supplies the demultiplexer 5C through the dual OR-gate 7C which over-rides the signals $a_{11}$, $b_{11}$ when the short answer (answer formal $F_1$) is required.

The outputs 1 to 8 of demultiplexer 5C

provide the word synchronisation necessary for the generation of the answer message; the output 1 also provides the slow clock which is sent to the counter in order to generate the answer delay. The beginning and the duration of the counting is controlled by the AND-gate 14C which is controlled by the R/S bistable 11C. This bistable is set to the logic state 1 by $F_1$ or $F_2$ through the OR-gate 9C, and to the logic state 0 by the reset signal A or by the appearance of the answer window J through the OR-gate 13C. The counter 16C comprises five sections serially connected.

Referring to Figure 8, the counter receives the slow clock through the gate 14C, and after having counted up to a number of pulses equal to the number set up therein (2054 in the case of Figure 8), it sets the R/S bistable 10C to the logic state 1 through the AND-gate 15C. This bistable 10C provides at its output the answer window, the duration of which is made dependent on the presence of $F_1$ or $F_2$, through the switch 6C.

The characteristic number of the subscriber (2054 in the case of Figure 8) is set up as follows:—

Figure 9a shows a printed circuit card corresponding to one section of the counter. Each section has a decade counter and a decoder which recognises the state of the four bistables forming the decade counter corresponding to the number impressed on the card. Four contacts of the card are connected so as to repeat in an excess three code the number impressed on the card thus providing the answer message generator with the subscriber's address.

By arranging side by side five such cards (Figure 9b) a complete counter is formed, which counts pulses of the slow clock and can accommodate subscribers' numbers (addresses) ranging from 1 to 99,999.

Figure 10 shows in greater detail the "answer message generator". Eight multiplexers 1D to 8D each having eight inputs and one output are provided. They are all simultaneously controlled by the bit synchronisation (a, b, c) and each of them is also individually controlled by a pulse with an 8-bit duration which acts as word synchronisation.

The inputs of the multiplexers are connected as follows:—

inputs 1—4 of multiplexer 1D are wired to form the starting sequence 1010;

inputs 5—8 of multiplexer 1D and inputs 1—4 of multiplexer 2D are wired so as to form the message beginning sequence 01111110;

inputs 5—8 of multiplexer 2D receive data from the keyboard;

inputs 1—4 of multiplexer 3D receive the data on some television channels tuned by the subscriber and for which taxed programmes are foreseen;

inputs 5—8 of multiplexer 3D receive from matrix 12D data repeating the command $B_1$ to $B_8$ received from the central unit;

inputs 1—8 of multiplexer 4D and of multiplexer 5D receive from external equipments data to be transmitted (reading of the meters; alarms, etc.);

input 1 of multiplexer 6D represents the parity bit relating to the data manually set up by the subscriber on the keyboard;

input 2 of multiplexer 6D represents the parity bit relating to the data on the TV channel received by the subscriber;

input 3 of multiplexer 6D represents the parity bit relating to the repetition of the received command ($B_1$ to $B_8$);

input 4 of multiplexer 6D represents the parity bit of the data coming from external equipments. The first three parity bits are obtained from circuit 11D, the fourth bit is supplied by the same external equipments generating the data to be transmitted;

inputs 5—8 of multiplexer 6D, inputs 1—8 of multiplexer 7D and inputs 1—8 of multiplexer 8D receive the subscriber's address generated in the subscriber counter.

All circuits described and shown in Figures 5 to 10 utilise commercially available integrated circuits.

WHAT WE CLAIM IS:—

1. A method of establishing two-way electrical communication in a cable television system between a central unit and subscriber terminals, the method comprising:—

(i) transmitting information in the form of a data stream from the central unit to a plurality of subscriber terminals simultaneously, the data stream including timing information for establishing a fast clock and a slow clock at each terminal, the slow clock having a period which is a multiple of the fast clock period, the data stream also including a reset signal, an answer format signal, and command signals;

(ii) at a subscriber terminal receiving the data stream, identifying the reset signal, delaying the data stream, and counting pulses of the slow clock starting from the answer format signal to generate a time delay characterising the said terminal;

(iii) generating, at a keyboard associated with the said terminal, a subscriber's answer to information in the received data stream; and

(iv) transmitting the answer from the said terminal to the central unit, the time interval between the receiving of the reset signal and the transmitting of the answer

being determined by the characteristic time delay,

each subscriber terminal having a different time delay assigned to it such that answers from the terminals are received at the central unit one after another in time-division-multiplexed form.

2. A method according to Claim 1, wherein the slow clock is synchronised by a repetitive synchronising word transmitted in the data stream, the words between first and second specified synchronising words being used to carry private communication data from the central unit to each subscriber, the first specified synchronising word being the synchronising word which completes the count of that subscriber terminal and the second being the next synchronising word.

3. A method according to Claim 1 or Claim 2, wherein the data stream transmitted from the central unit to each subscriber terminal and the answers transmitted from the subscriber terminal to the central unit are respectively transmitted on two different cables.

4. A method according to Claim 1 or Claim 2, wherein the data stream transmitted from the central unit to each subscriber terminal and the answers transmitted from the subscriber terminal to the central unit are transmitted on a single cable using two coded modulated signals having different carrier frequencies.

5. A subscriber terminal device connectable to a cable television system for two-way electrical communication, in which system a data stream having a fast clock bit time interval and including synchronising words at a slow clock interval, a reset signal, an answer format signal, and command signals are generated at a central unit and are transmitted to the terminal device, answers from the terminal device being received by the central unit, the terminal device comprising:—

first regenerator means for regenerating the fast clock pulses;

shift register means controlled by said first regenerator means for receiving the data stream from the central unit and generating a delay corresponding to the expression $2(T_{max}-T_J)$, wherein $T_{max}$ is the time taken for the data stream from the central unit to reach a remote subscriber, and $T_J$ is the time to reach the particular terminal device;

word decoder means connected to the output of said shift register means;

second regenerator means controlled by said shift register means for regenerating slow clock pulses;

counter means for receiving said slow clock pulses and for counting up to a number J assigned to that terminal device, said counter means beginning the count of slow clock pulses when the answer format signal from the central unit is received and decoded by said word decoder means; and

keyboard means for entry thereon of answer data, said counter means producing an output gate upon reaching the count of said number J for enabling the transmission of the answer data from the terminal device.

6. A device according to Claim 5 when connected to the system;

wherein the incoming data stream from the central unit is continuous, is organised in 8-bit words, each word being encoded by employing those code combinations having two or four bits with logic value 1, except for the combinations 11000000, 00000011, 11110000, 00001111, and has a period of nine words, the beginning of which period is represented by the code word 01111110;

and wherein said word decoder means comprises:— first and second serially connected shift registers, having respectively 64 and 8 delay stages, which registers feed a first diode matrix, a parity check circuit and separator means, the latter being connectable to external equipment; an "EXCLUSIVE OR" circuit connected to receive signals from the input of the first shift register and from the last output of the second shift register, the output of the said "EXCLUSIVE OR" circuit being connected to the input of a third shift register comprising seven delay stages; an "AND" gate connected to receive signals from the outputs of the third shift register and the output of the parity check circuit; and a second diode matrix connected to receive signals from the output of the "AND" gate, from the output of the parity check circuit and from the outputs of the second shift register, for decoding the words and commands of the incoming data stream; the word decoder further comprising bistable flip/flops of the set/reset type for storing the decoded commands.

7. A device according to Claim 6 comprising a bistable memory means for receiving the information from the second diode matrix means when the said output gate is open.

8. A device according to Claim 5 including a plurality of removable units, each unit comprising a printed circuit card having a plurality of contacts and containing a decade and decoding means; said decoding means including four bistable flip-flops and being preset to identify that state of the four flip-flops which coincides, in the employed code, with the number assigned to the card; four of said contacts being wired to represent, in the employed

code, the number assigned to the card; said counter means being formed by the combination of two or more of said cards connected in series, the first card being controlled by the slow clock; the said cards further including means for changing the number assigned to the terminal.

9. A method of establishing two-way electrical communication in a cable television system between a central unit and subscriber terminals, the method being substantially as herein described with reference to the drawings.

10. A subscriber terminal device connectable to a cable television system for two-way electrical communication, the device being constructed and arranged substantially as herein described and shown in the accompanying drawings.

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FIG. 1

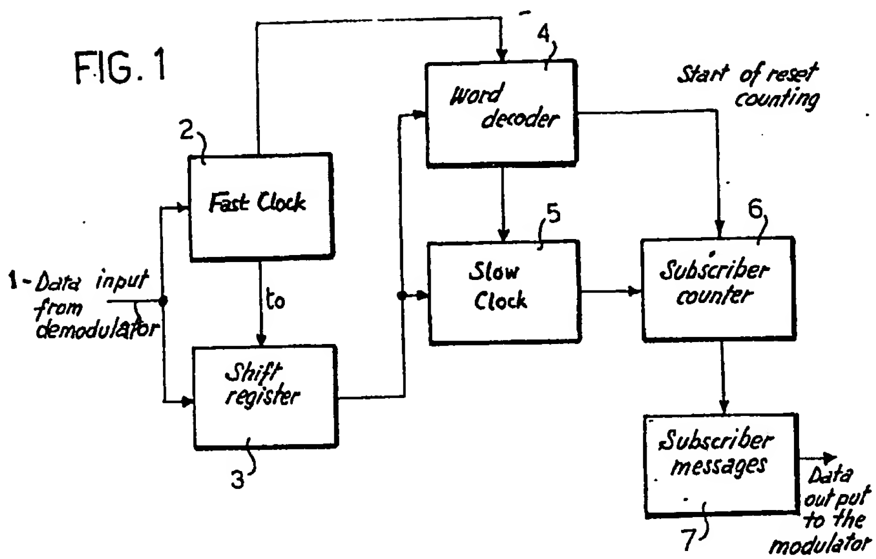
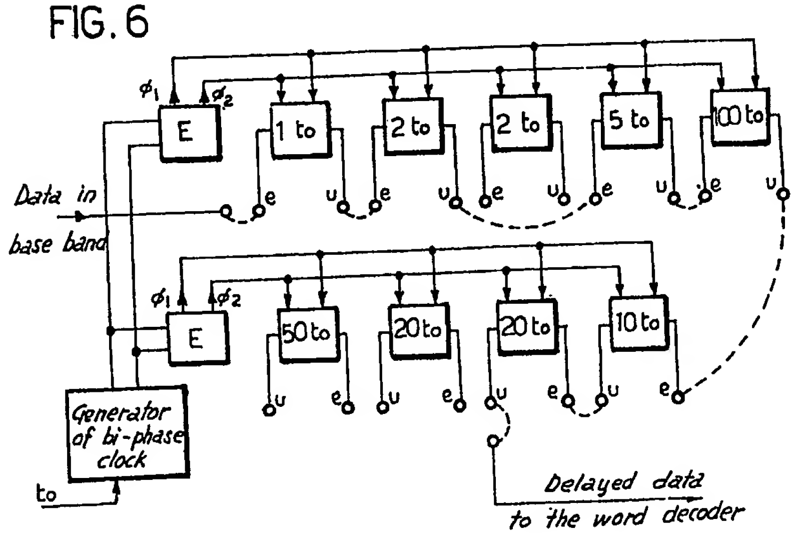

Word decoder
Start of reset counting
Fast Clock
to
1-Data input from demodulator
Slow Clock
Subscriber counter
Shift register
Subscriber messages
Data output to the modulator
2
3
4
5
6
7

FIG. 6


E
1 to
2 to
2 to
5 to
100 to
Data in base band
E
50 to
20 to
20 to
10 to
Generator of bi-phase clock
to
Delayed data to the word decoder

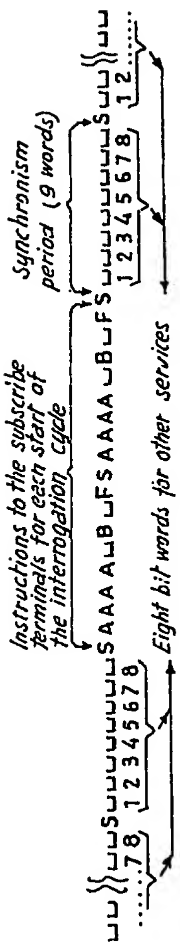



FIG. 2

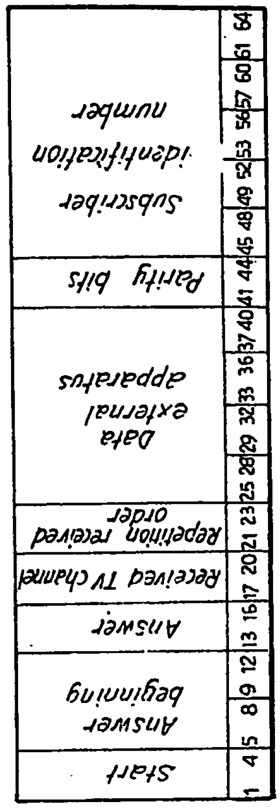



FIG. 4

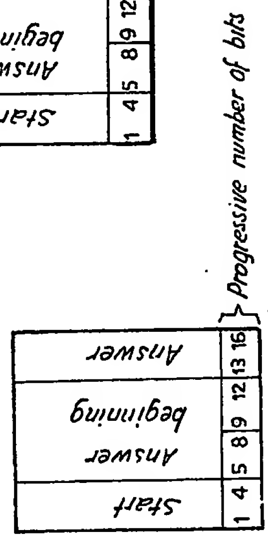



FIG. 3

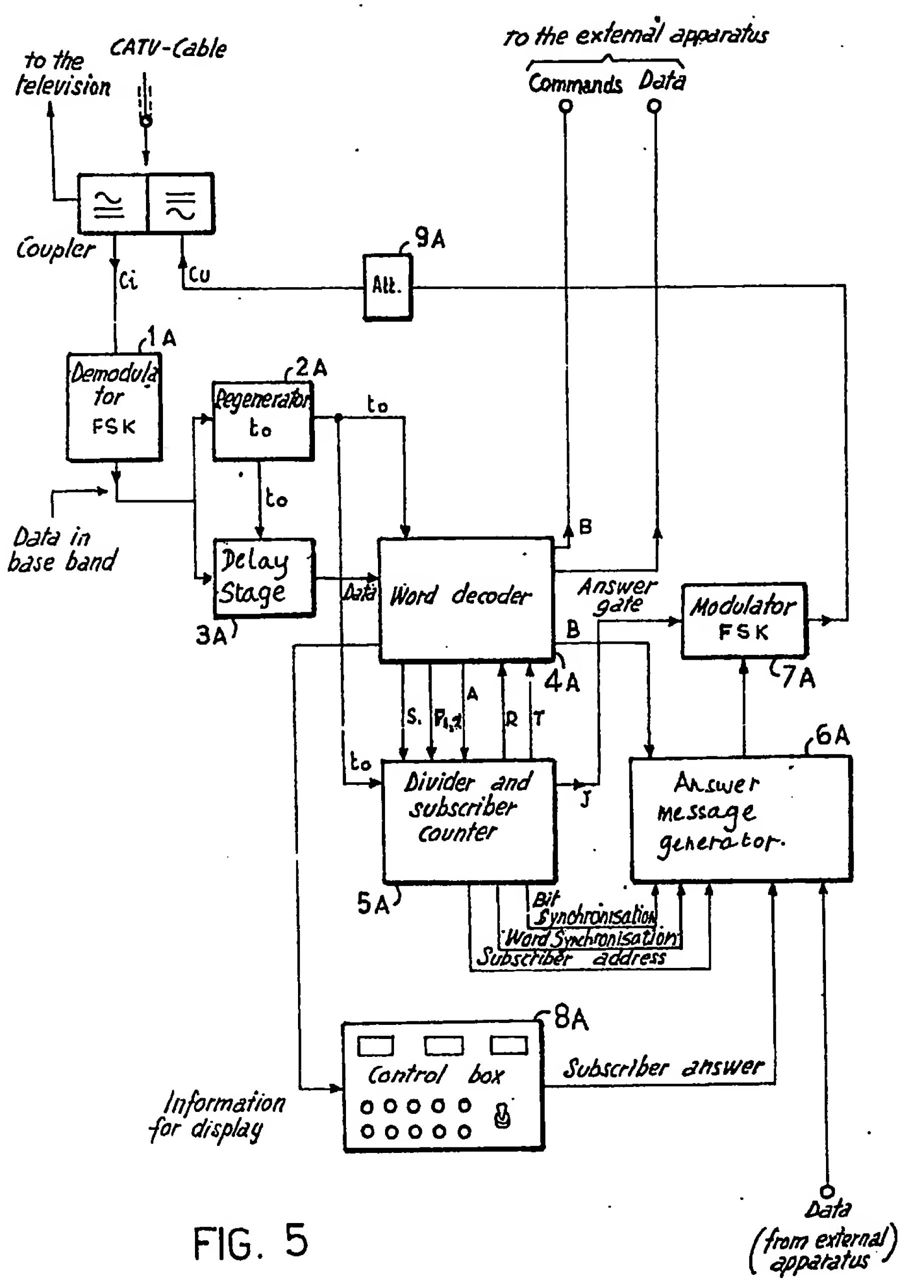

to the television
CATV-Cable
To the external apparatus
Commands
Data
Coupler
Ci
Cu
9A
Alt.
1A
Demodulator FSK
2A
Regenerator $t_0$
$t_0$
Data in base band
Delay Stage
3A
Data
Word decoder
4A
B
Answer gate
Modulator FSK
7A
S.
A
R
T
6A
Divider and subscriber counter
5A
J
Answer message generator.
Bit Synchronisation
Word Synchronisation
Subscriber address
8A
Control box
Subscriber answer
Information for display
Data (from external apparatus)

FIG. 5

FIG. 7

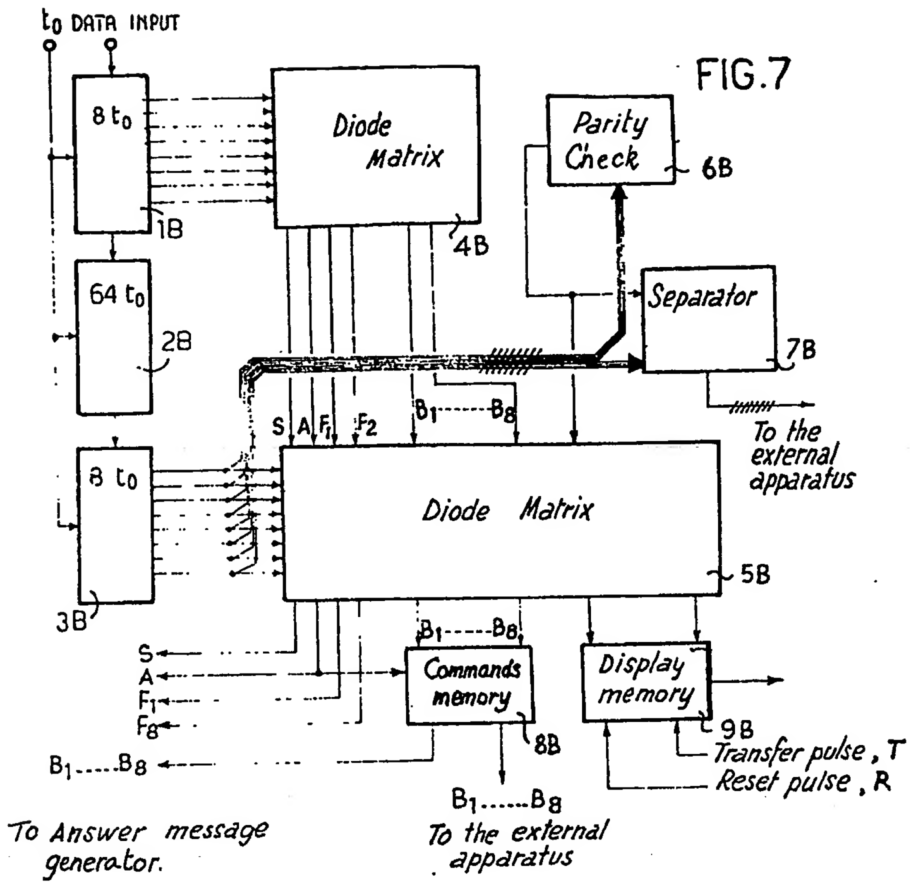



FIG. 9a

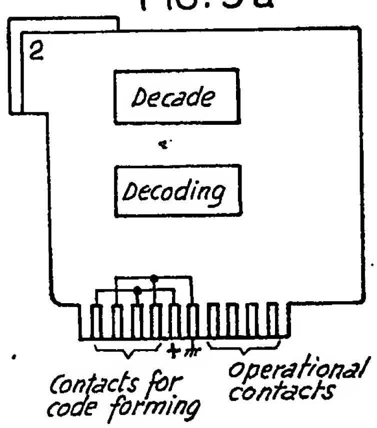
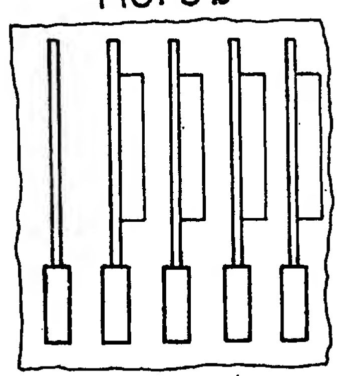



FIG. 9b



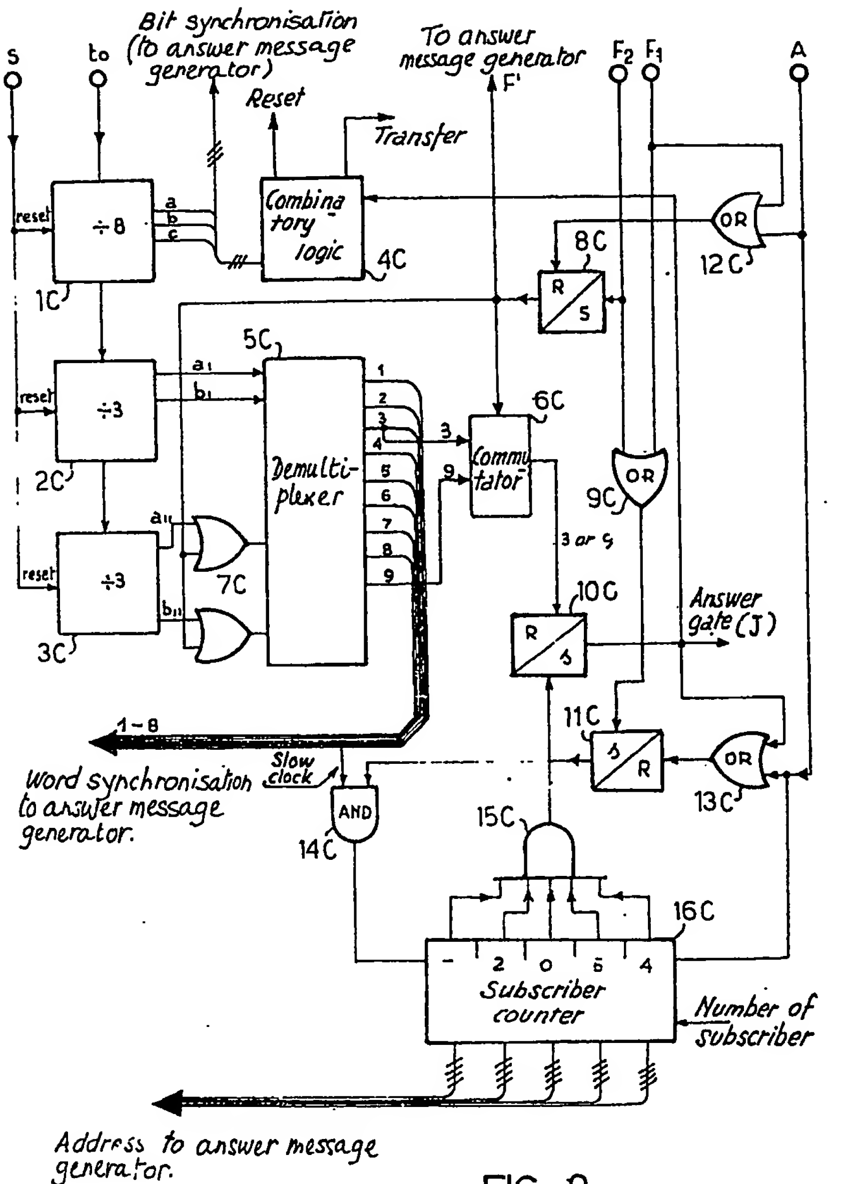

S
to
Bit synchronisation (to answer message generator)
Reset
Transfer
To answer message generator
F'
$F_2$
$F_1$
A
reset
÷8
a
b
c
1C
Combinatory logic
4C
8C
R
S
OR
12C
5C
$a_1$
$b_1$
÷3
2C
Demultiplexer
6C
Commutator
3 or 9
OR
9C
$a_{11}$
$b_{11}$
÷3
3C
7C
10C
Answer gate (J)
11C
OR
13C
1-8
Word synchronisation to answer message generator.
Slow clock
AND
14C
15C
16C
Subscriber counter
Number of subscriber
Address to answer message generator.

FIG. 8

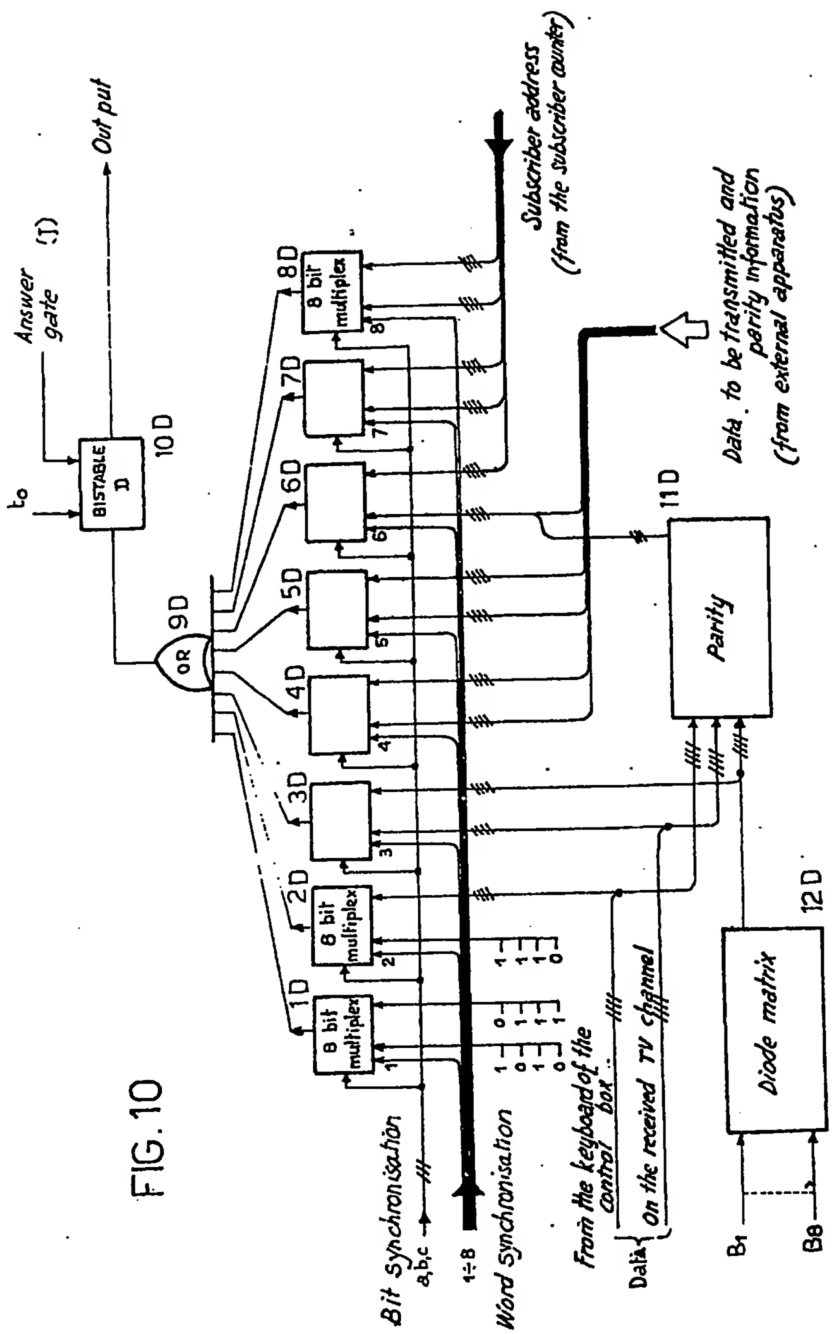

Answer gate
(J)
Out put
$t_o$
BISTABLE D
10D
OR
9D
8 bit multiplex
1D
2D
3D
4D
5D
6D
7D
8D
Subscriber address (from the subscriber counter)
Data to be transmitted and parity information (from external apparatus)
11D
Parity
Diode matrix
12D
Bit synchronisation a,b,c
1÷8
Word synchronisation
From the keyboard of the control box
On the received TV channel
Data
B1
B8

FIG. 10